AMENDMENTS TO THE CLAIMS

Amendment to the Claims

1-67. (Cancelled)

68. (Currently Amended) A process for electrochemical deposition of metal onto a surface of a microelectronic workpiece ~~including at least one low-K dielectric layer~~, comprising:

exposing a surface of the microelectronic workpiece to a plating solution including a principal metal species to be deposited;

applying plating power between the surface of the workpiece and an electrode disposed in contact with the plating solution to electrolytically deposit metal onto the surface, wherein plating power is applied

at a first current density for a first period of time to deposit a first ~~layer~~ amount of the metal onto the surface of the workpiece, and subsequently

at a second current density for a second period of time to deposit a second ~~layer~~ amount of the metal onto the first ~~layer~~ amount of metal, wherein the second current density is ~~substantially~~ greater than the first current density and a majority of the metal deposited onto the surface of the workpiece is deposited during the second time period; and

subjecting the surface of the microelectronic workpiece to an elevated temperature annealing process at a predetermined temperature ~~that is below a temperature at which the low-K dielectric layer would substantially degrade~~.

69. (Previously Presented) The process of Claim 68, wherein the surface of the microelectronic workpiece defines a plurality of recessed microstructures, and the

first current density and first period of time are selected to at least partially fill the recessed microstructures with the deposited metal.

70. (Previously Presented) The process of Claim 68, wherein metal deposited during the first time period has a grain size that is sufficiently small to fill the recessed microstructures and at least some of the recessed microstructures have a width of less than or equal to 0.3 micron.

71. (Currently Amended) The process of Claim 68, wherein the metal is annealed at a temperature of ~~at or~~ below about 250° C.

72. (Previously Presented) The process of Claim 68, wherein the first current density is about 3.2 mA/cm^2

73. (Previously Presented) The process of Claim 68, wherein the second current density is about 20 mA/cm^2

74. (Previously Presented) The process of Claim 68, wherein a ratio of the second current density to the first current density is about 6:1.

75. (Previously Presented) The process of Claim 68, wherein the first time period is about 30 seconds.

76. (Currently Amended) The process of Claim 68, wherein the metal is annealed at a temperature of ~~at or~~ below about ~~250° C to~~ 300° C.

77. (Previously Presented) The process of Claim 68, wherein metal is deposited at a higher rate during the second time period than during the first time period.

78. (Previously Presented) The process of Claim 68, further comprising depositing a seed layer onto the surface of the microelectronic workpiece prior to the first time period, the first layer of metal being deposited onto the seed layer.

79. (Previously Presented) The process of Claim 68, wherein the principal metal species deposited comprises copper.

80. (Currently Amended) A process for electrochemical deposition of copper onto a surface of a microelectronic workpiece, comprising:

exposing a surface of the microelectronic workpiece to a plating solution including copper as a principal metal species to be deposited;

applying plating power between the surface of the workpiece and an electrode disposed in contact with the plating solution to electrolytically deposit copper onto the surface, wherein plating power is applied

at a first current density for a first period of time to deposit a first ~~layer~~ amount of copper onto the surface of the workpiece, and subsequently

at a second current density for a second period of time to deposit a second ~~layer~~ amount of copper onto the first ~~layer~~ amount of copper, wherein the second current density is ~~substantially~~ greater than the first current density and a majority of copper deposited onto the surface of the workpiece is deposited during the second time period; and

subjecting the surface of the microelectronic workpiece to an elevated temperature annealing process at a predetermined temperature that is below about 300° C.

81. (Previously Presented) The process of Claim 80, wherein the second current density is applied immediately after the first period of time.

82. (Currently Amended) A process for electrochemical deposition of metal onto a surface of a microelectronic workpiece, the surface defining a plurality of recessed microstructures, the workpiece including at least one low-K dielectric layer, comprising:

exposing a surface of the microelectronic workpiece to a plating solution including a principal metal species to be deposited;

applying plating power between the surface of the workpiece and an electrode disposed in contact with the plating solution to electrolytically deposit metal onto the surface, wherein plating power is applied

at a first current density for a first period of time to deposit a first layer of the metal onto the surface of the workpiece to at least partially fill the recessed microstructures, and subsequently

at a second current density for a second period of time to deposit a second layer of the metal onto the first layer of metal, wherein the second current density is ~~substantially~~ greater than the first current density; and

subjecting the surface of the microelectronic workpiece to an elevated temperature annealing process at a predetermined temperature that is below a temperature at which the low-K dielectric layer would substantially degrade.

83. (Previously Presented) The process of Claim 82, wherein the second current density is applied immediately after the first period of time has elapsed.

84. (Currently Amended) A process for electrochemical deposition of metal onto a surface of a microelectronic workpiece~~, the workpiece including at least one low-K dielectric layer~~, comprising:

applying a metal seed layer onto a surface of the microelectronic workpiece;

exposing the surface of the microelectronic workpiece to a plating solution including a principal metal species to be deposited;

applying plating power between the surface of the workpiece and an anode disposed in contact with the plating solution to electrolytically deposit metal onto the surface, wherein plating power is applied

at a first current density for a first period of time to deposit a first ~~layer~~ amount of the metal onto the seed layer on the surface of the workpiece, and subsequently

at a second current density for a second period of time to deposit a second ~~layer~~ amount of the metal onto the first ~~layer~~ amount of metal, wherein the second current density is ~~substantially~~ greater than the first current density; and

subjecting the surface of the microelectronic workpiece to an elevated temperature annealing process at a predetermined temperature ~~that is below a temperature at which the low-K dielectric layer would substantially degrade~~.

85. (Currently Amended) A method of depositing a metal layer on a semiconductor wafer~~, the workpiece including at least one low-K dielectric layer~~, comprising:

depositing a seed layer on a surface of the wafer;

immersing the wafer in an electrolytic solution containing metal ~~innsions~~ions;

electrolytically depositing a first plated layer on the wafer by applying current at a first current density between the wafer and the solution;

after a first period of time during which the first plated layer has been formed, increasing the applied current to a second current density greater than the first current density to plate additional metal onto the first plated layer; and

subjecting the surface of the microelectronic workpiece to an elevated temperature annealing process at a predetermined temperature~~ that is below a temperature at which the low-K dielectric layer would substantially degrade~~.

86-106. (Cancelled)

107. (New) The process of Claim 85, wherein the surface of the microelectronic workpiece defines a plurality of recessed microstructures, and the first current density and first period of time are selected to at least partially fill the recessed microstructures with the deposited metal.

108. (New) The process of Claim 85, wherein metal deposited during the first time period has a grain size that is sufficiently small to fill the recessed microstructures and at least some of the recessed microstructures have a width of less than or equal to 0.3 micron.

109. (New) The process of Claim 85, wherein the metal is annealed at a temperature of below about 250° C.

110. (New) The process of Claim 85, wherein the first current density is about 3.2 mA/cm^2

111. (New) The process of Claim 85, wherein the second current density is about 20 mA/cm^2

112. (New) The process of Claim 68, wherein a ratio of the second current density to the first current density is about 6:1.

113. (New) The process of Claim 85, wherein the first time period is about 30 seconds.

114. (New) The process of Claim 85, wherein the metal is annealed at a temperature of below about 300° C.

115. (New) The process of Claim 85, wherein metal is deposited at a higher rate during the second time period than during the first time period.

116. (New) The process of Claim 85, further comprising depositing a copper seed layer onto the surface of the microelectronic workpiece prior to the first time period, the first layer of metal being copper deposited onto the seed layer.

117. (New) The process of Claim 85, wherein the principal metal species deposited comprises copper.